

FIG. 1A
(PRIOR ART)

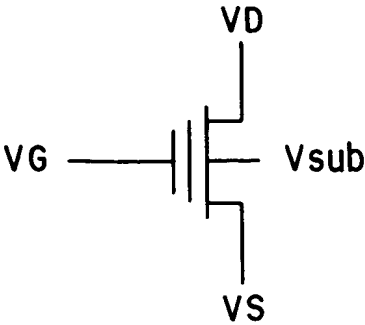


FIG. 1B
(PRIOR ART)

	VD	VG	VS	Vsub
READ	1 V	5 V	0 V	0 V
WRITE	5 V	10 V	0 V	0 V
ERASURE	OPEN	-7 V	6 V	0 V

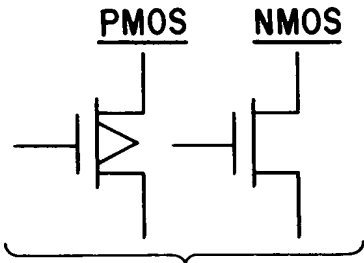


FIG. 2A
(PRIOR ART)

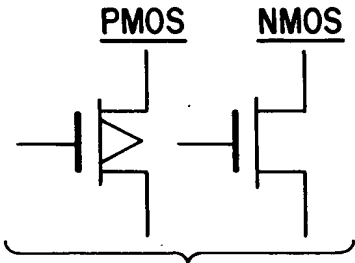
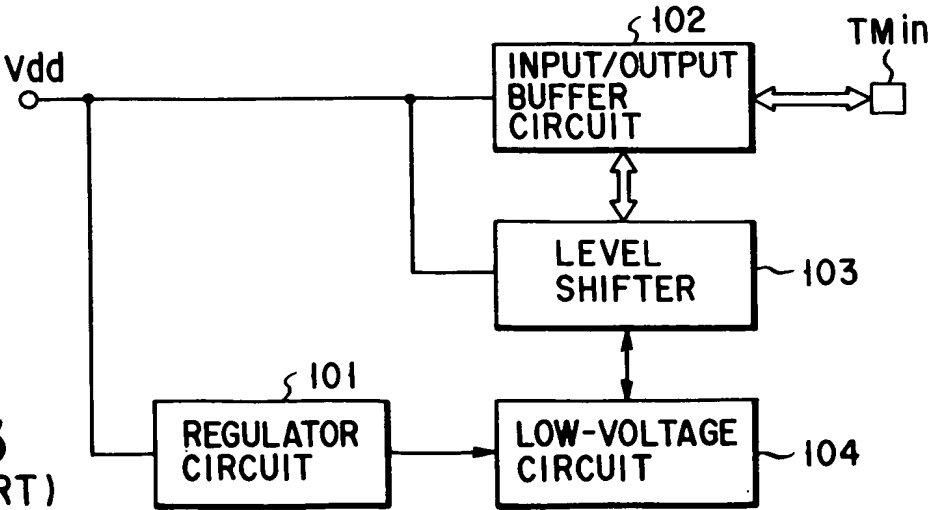


FIG. 2B
(PRIOR ART)

FIG. 3
(PRIOR ART)



APPROVED	O.G. FIG.	
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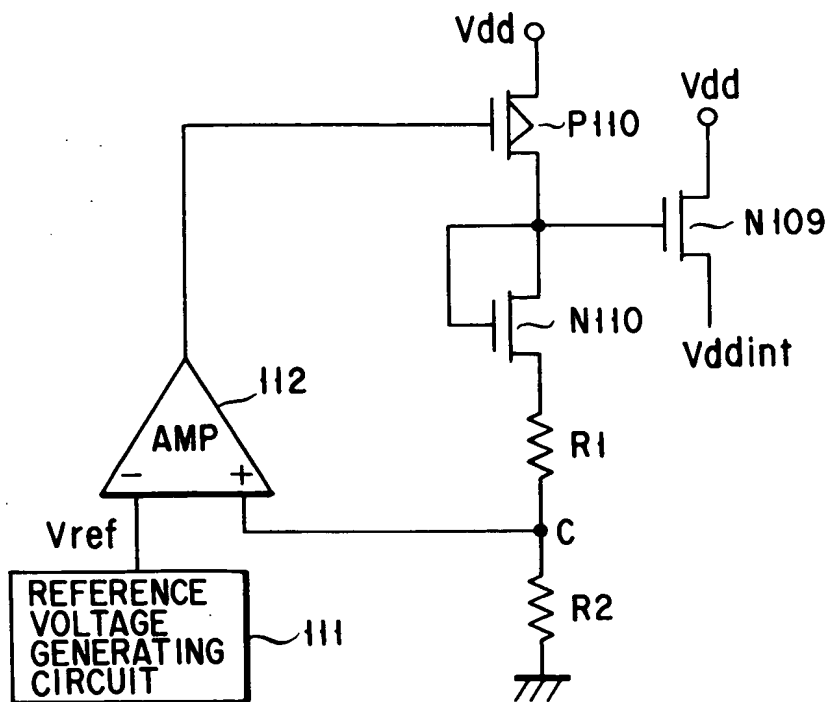


FIG. 4 (PRIOR ART)

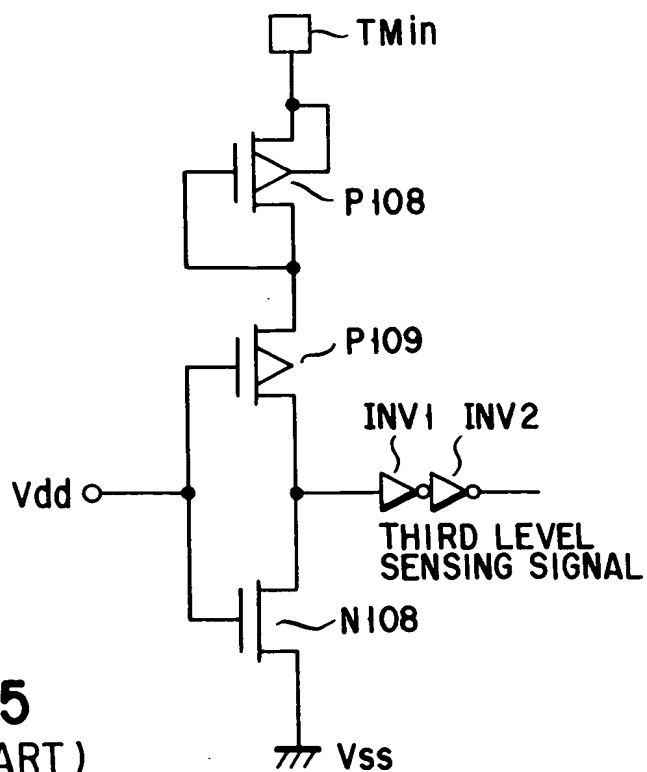


FIG. 5
(PRIOR ART)

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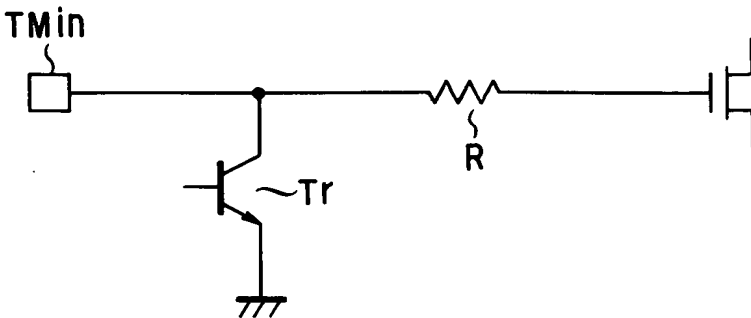


FIG. 6A
(PRIOR ART)

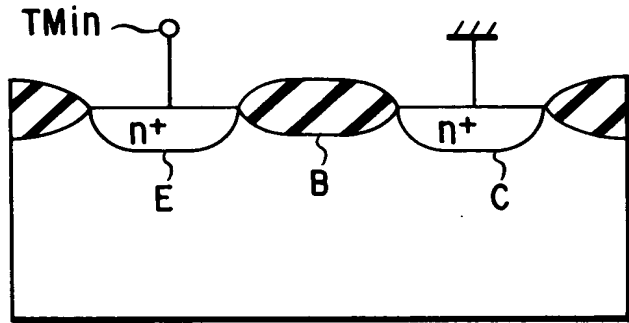


FIG. 6B
(PRIOR ART)

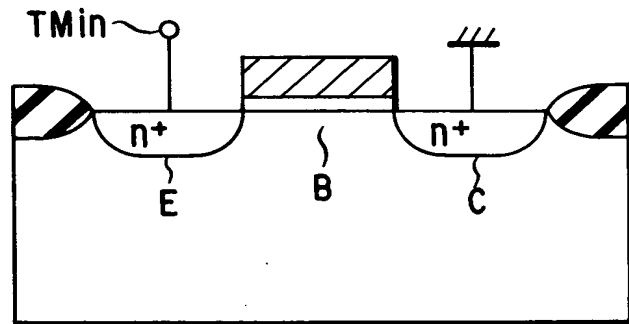


FIG. 6C
(PRIOR ART)

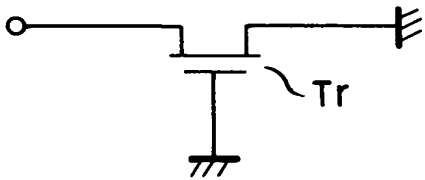


FIG. 6D
(PRIOR ART)

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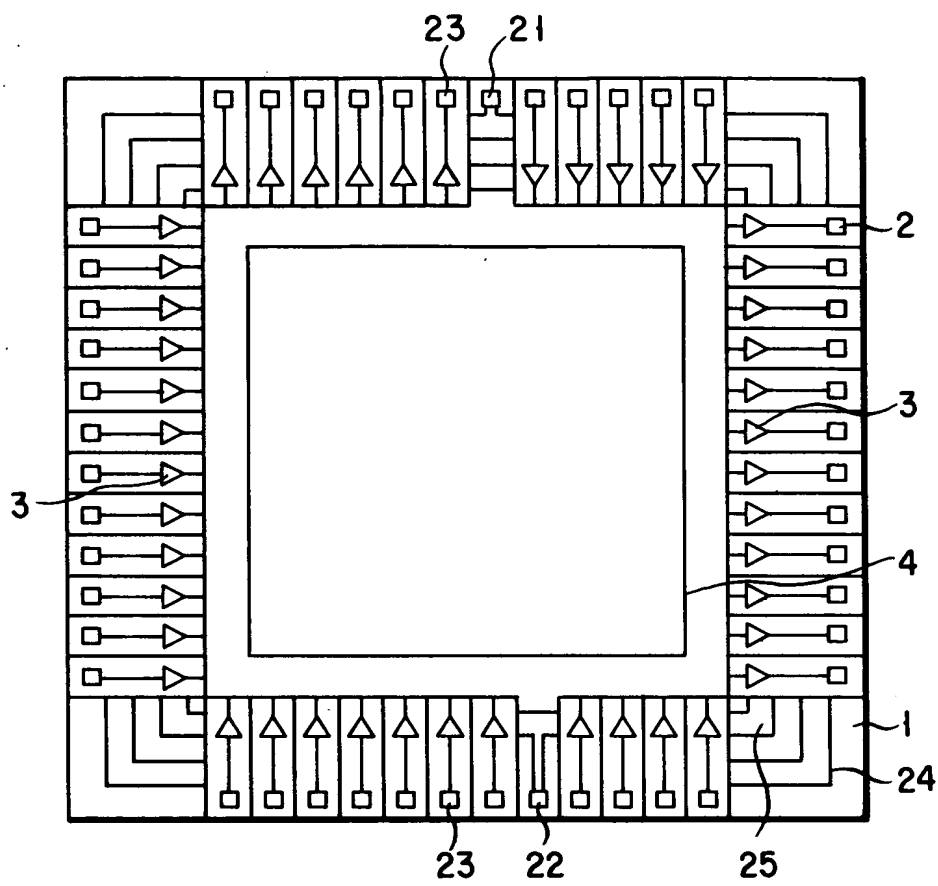


FIG. 7

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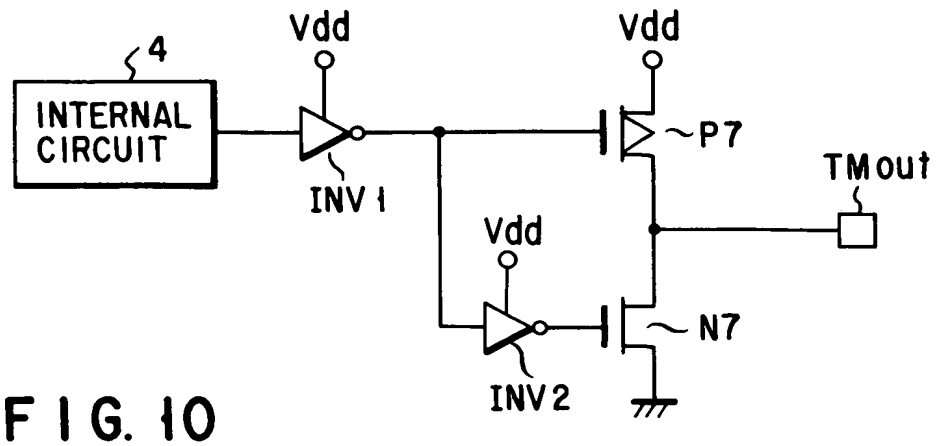


FIG. 10

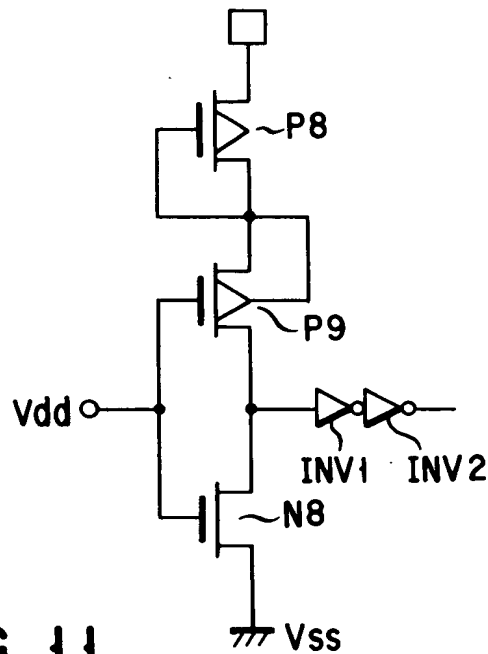


FIG. 11

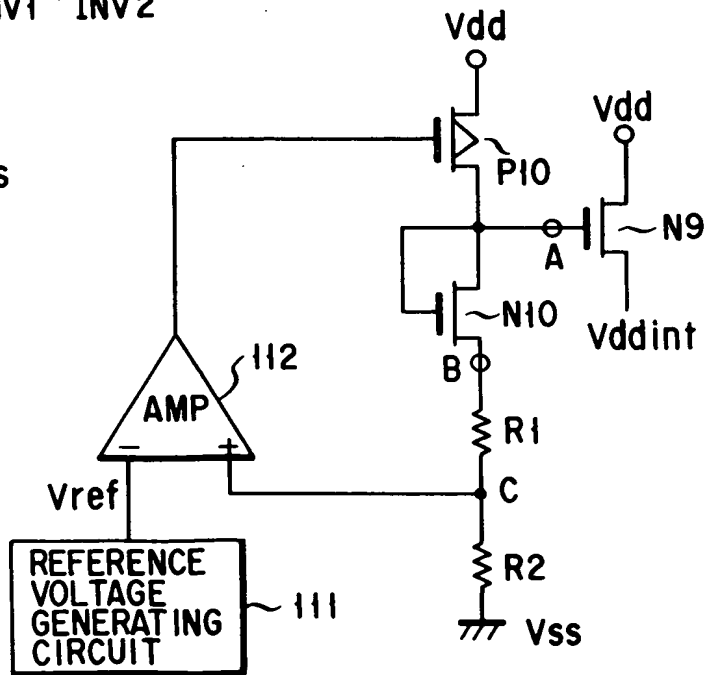
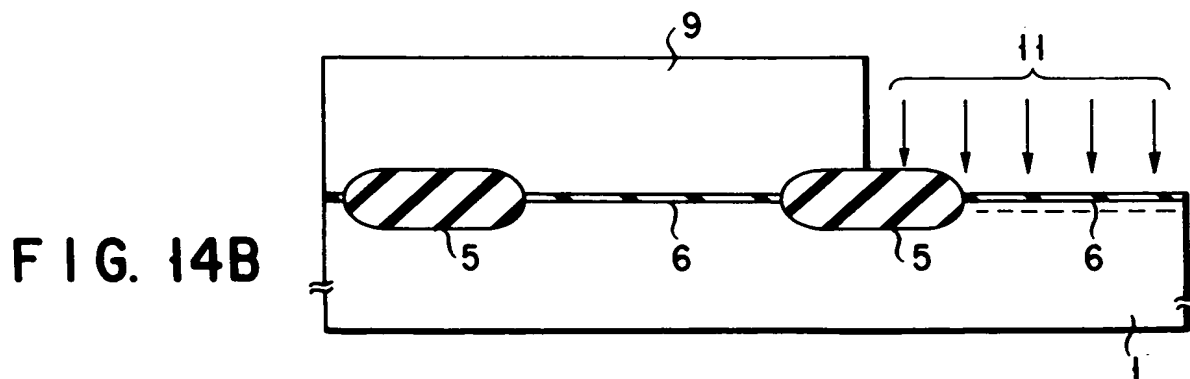
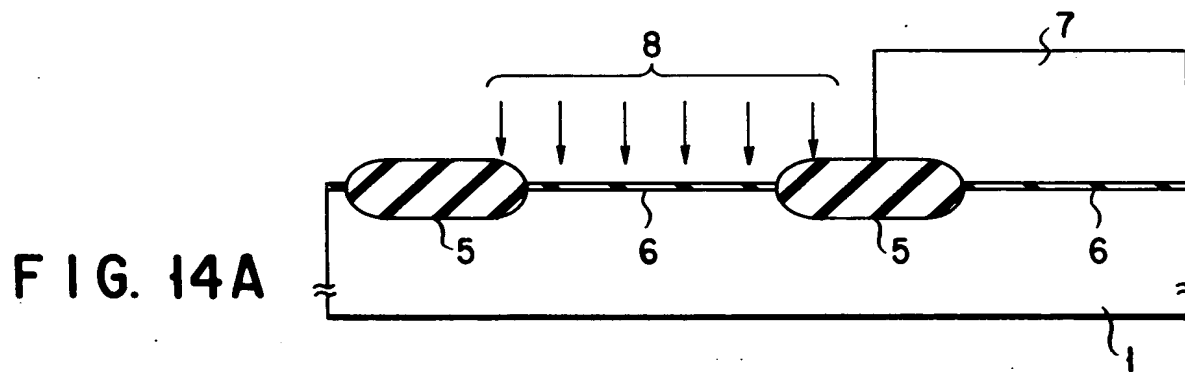
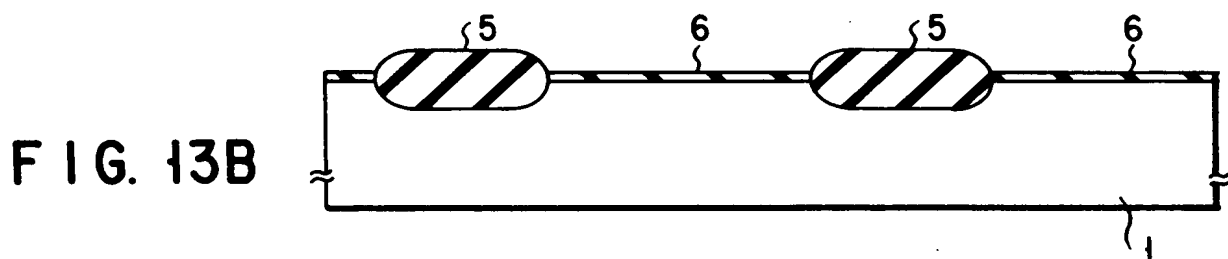
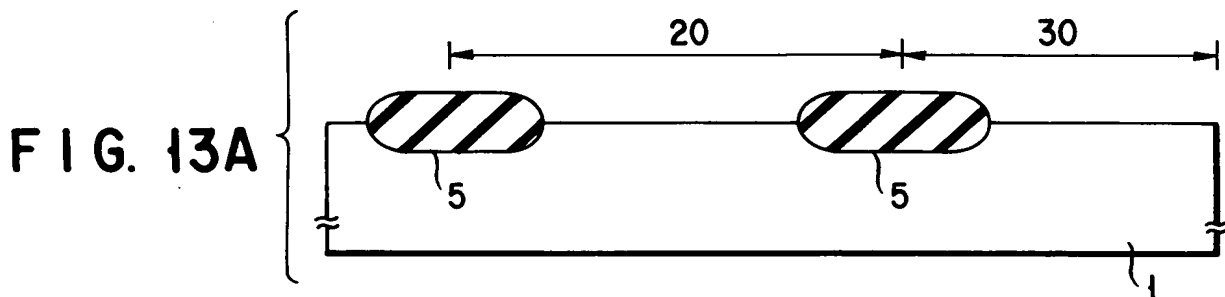
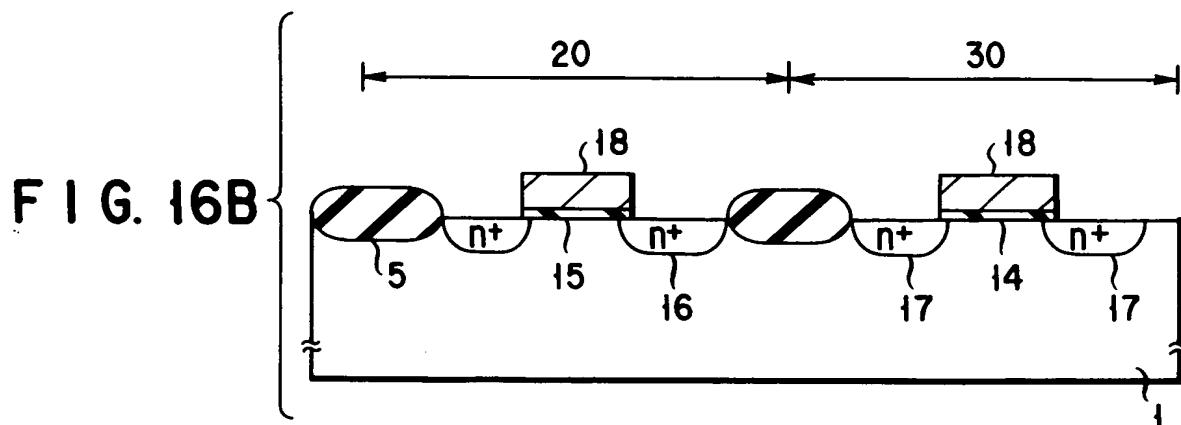
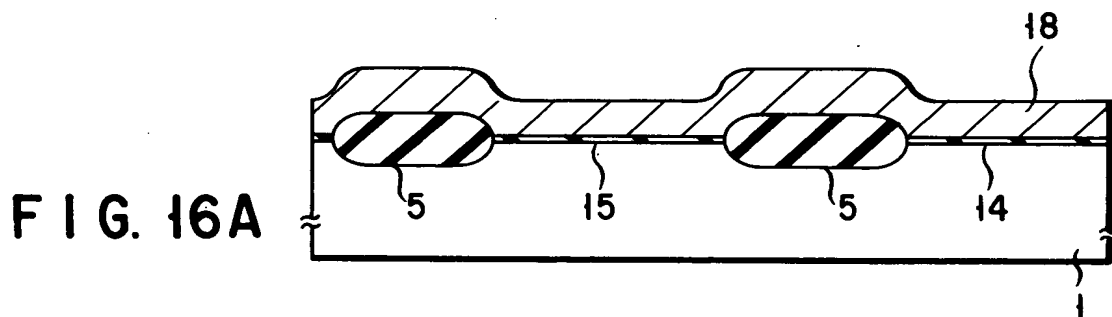
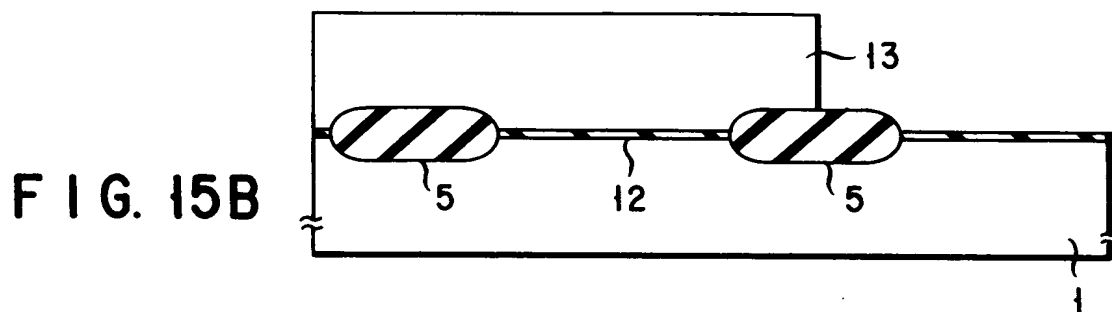
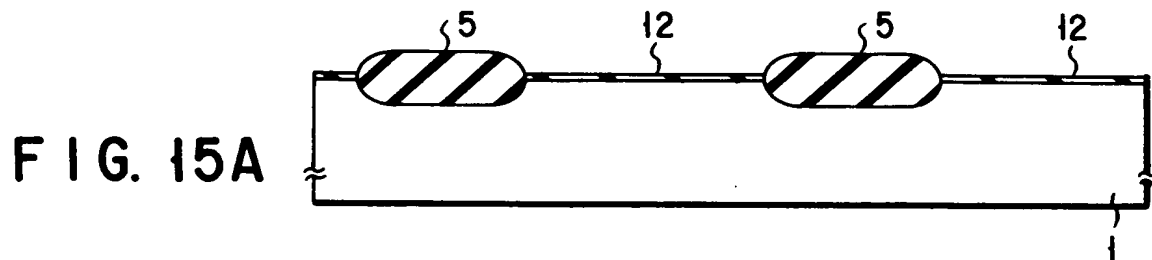


FIG. 12

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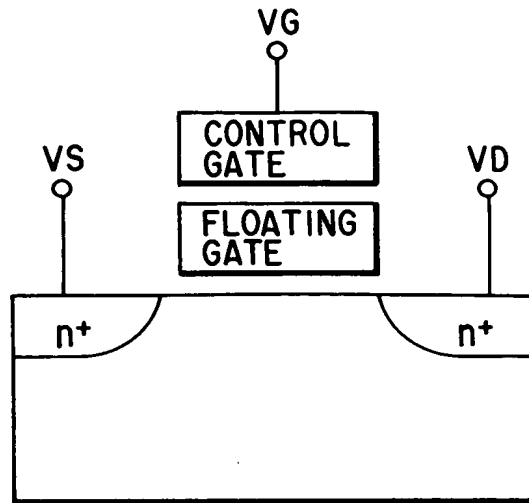


FIG. 17A

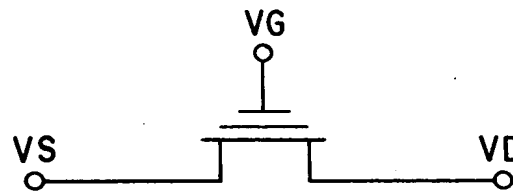


FIG. 17B

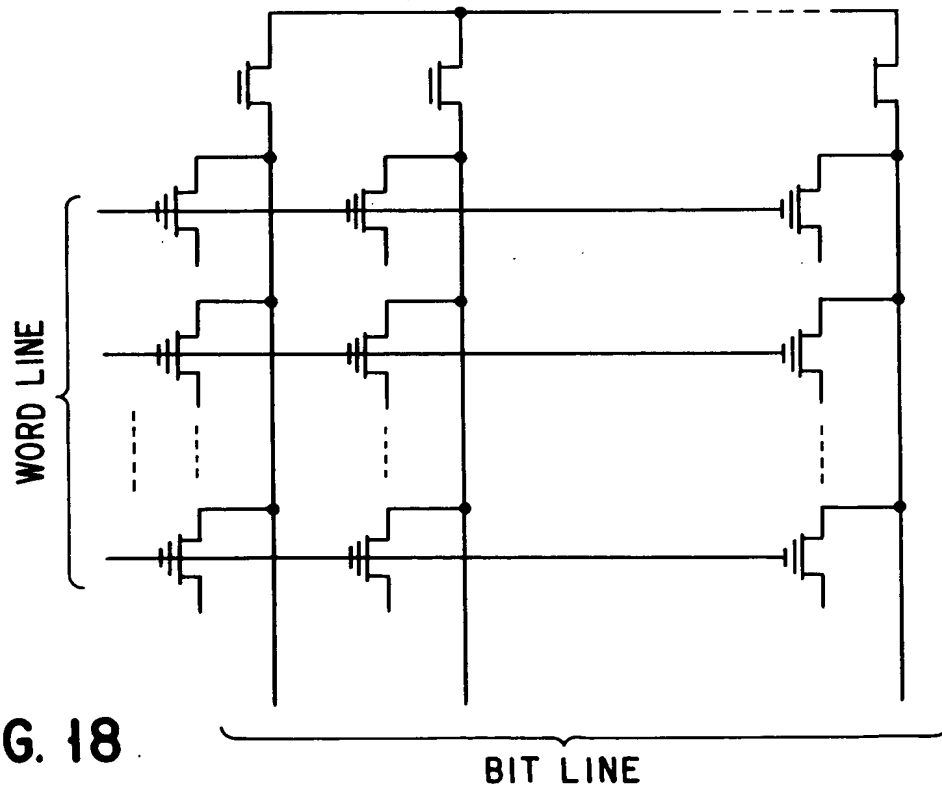


FIG. 18

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APPROVED	O.G. FIG.	
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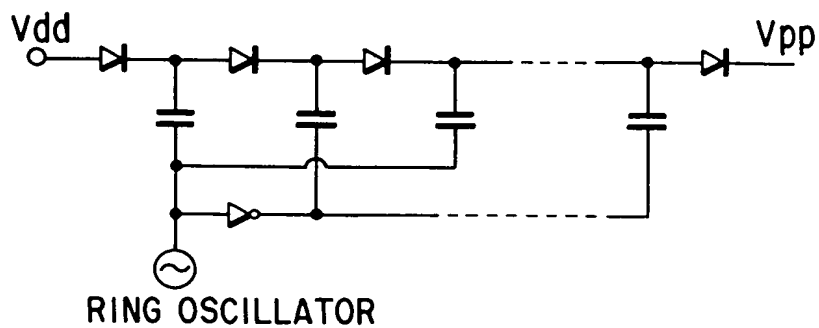
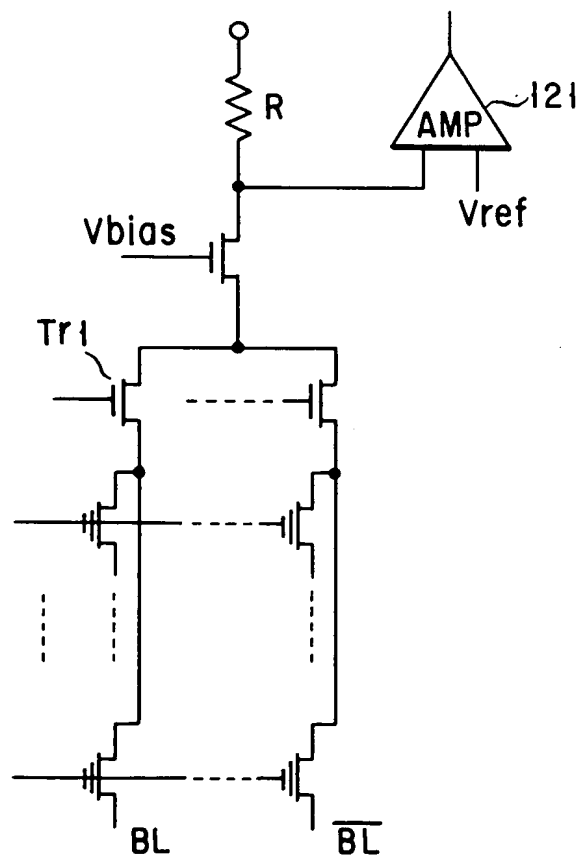


FIG. 19



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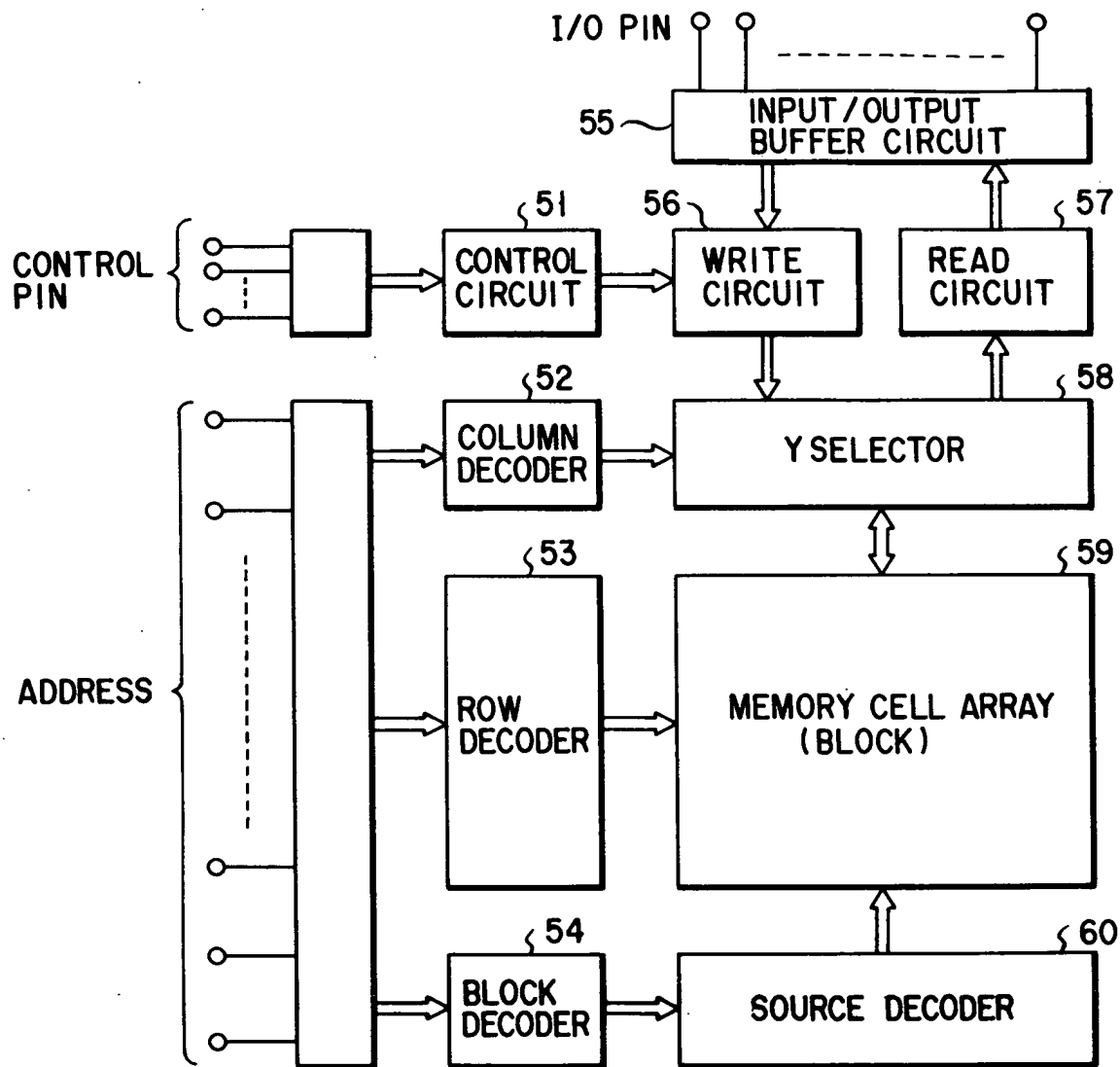


FIG. 21

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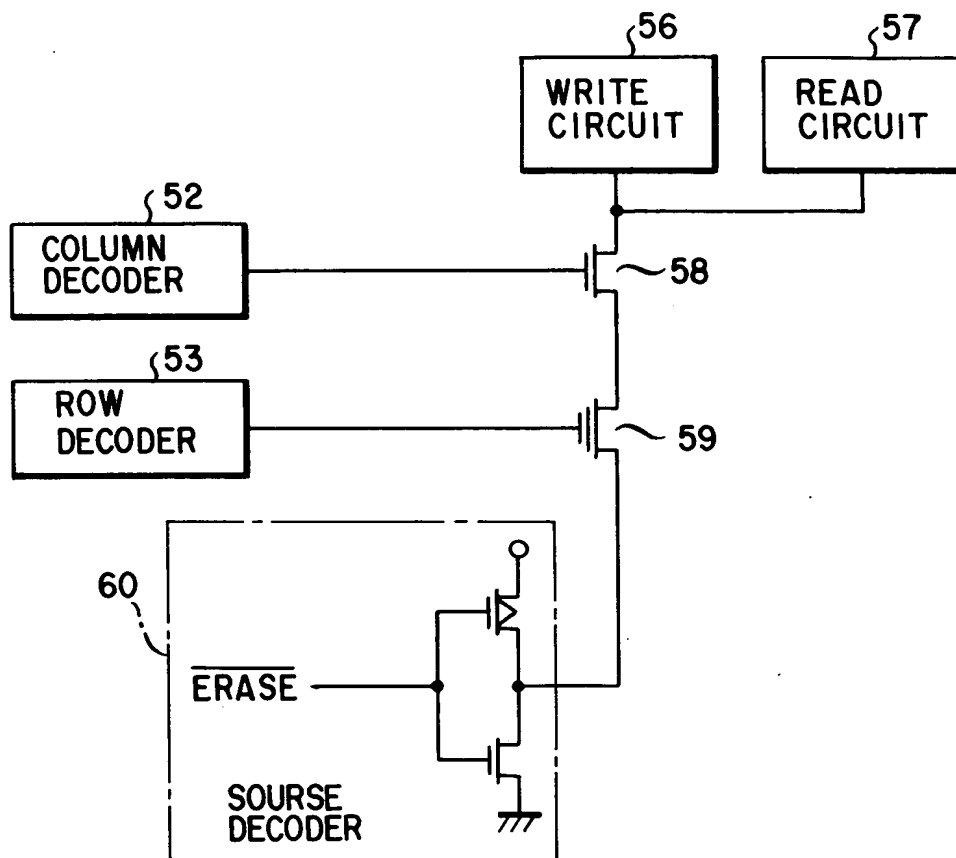


FIG. 22

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